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09/603,226	06/26/2000	Donald E. Steiss	TI-29338	3213

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	8

DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/603,226	STEISS ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 have been considered. Claims 1, 2, 10, and 11 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 7, 10, 12, and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., U.S. Patent Number 5,961,632 (herein referred to as Shiell) in view of O'Connor, U.S. Patent Number 5,848,288 (herein referred to as O'Connor).

4. Shiell has taught the structure of a subpipelined translation embodiment providing binary compatibility between a base architecture and migrant architecture comprising:

a. A base architecture and a migrant architecture and having a base execution mode and a migrant execution mode (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; and Figure 5);

b. An instruction fetch unit, the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; Figure 1; and Figure 5);

c. A shared datapath by both the base and migrant architectures for parsing said base architecture mode and migrant architecture mode fetch packets into execute packets of instructions within said fetch packet (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 3, lines 36-42; Figure 1; and Figure 5);

d. A base architecture control circuit for dispatching execute packet instructions having a base execution mode (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

e. A migrant architecture control circuit for dispatching execute packet instructions having a migrant execution mode (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

f. A base architecture decode connected to said shared datapath and said base architecture control circuit for decoding an execute packet in said base mode and generating a corresponding machine word (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 1; Figure 3a; Figure 3b; and Figure 5);

g. A migrant architecture decode connected to said shared datapath and said migrant architecture control circuit for decoding an execute packet in said migrant mode and generating a corresponding machine word (Shiell Abstract; column 1, line 61

to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 1; Figure 3a; Figure 3b; and Figure 5);

h. A multiplexer having at least two inputs and one machine word output wherein one input is the output of said migrant architecture decode and the other input is the output of said base architecture decode, said multiplexer choosing in dependence upon the operating mode of said fetch packet (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

i. Execute hardware connected to said multiplexer for executing execute packet instructions on execution units corresponding to said machine word chosen by said multiplexer (Shiell column 3, lines 27-46; Figure 1; Figure 3a; Figure 3b; and Figure 5).

5. Shiell has not explicitly taught a VLIW architecture comprising a base architecture and a migrant architecture and simultaneously fetching from memory a group of a plurality of instructions, each such group forming a fetch packet. However, Shiell has taught their system is usable with VLIW instruction sets (Shiell column 3, lines 36-42). O'Connor has taught a VLIW architecture comprising a base architecture and a migrant architecture (O'Connor column 1, line 9 to column 2, line 2) and simultaneously fetching from memory a group of a plurality of instructions, each such group forming a fetch packet (O'Connor column 1, line 9 to column 2, line 2). A person of ordinary skill in the art at the time the invention was would have recognized that using VLIW architecture improves code execution speed of the processor by executing more

than one instruction simultaneously (O'Connor column 1, lines 16-17) and allowing more than one type of VLIW instruction set to run improves compatibility of the processor with other programs by expanding the number of very long instructions recognized (O'Connor column 1, lines 60-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW architecture and simultaneous fetching of O'Connor in Shiell to improve processor speed and compatibility.

6. Referring to claims 3 and 12, Shiell has taught wherein said machine word also controls registers (Shiell column 3, lines 25-46)

7. Referring to claims 7 and 16, Shiell has taught wherein the base and migrant architecture decode units translates opcodes to the control signals required to execute the specified instructions on the execution hardware functional units (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5)

8. Referring to claim 10, Shiell has taught a method of providing binary compatibility between a base architecture and a migrant architecture comprising the steps of:

a. The fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; Figure 1; and Figure 5);

b. Parsing said base architecture mode and migrant architecture mode fetch packets into execute packets of instructions within said fetch packet (Shiell Abstract;

column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 3, lines 36-42; Figure 1; and Figure 5);

c. Dispatching execute packet instructions having a base execution mode (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

d. Dispatching execute packet instructions having a migrant execution mode (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

e. Decoding an execute packet in said base mode and generating a corresponding machine word (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 1; Figure 3a; Figure 3b; and Figure 5);

f. Decoding an execute packet in said migrant mode and generating a corresponding machine word (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 46; Figure 1; Figure 3a; Figure 3b; and Figure 5);

g. Choosing one machine word output, in dependent upon the operating mode of said fetch packet, between the machine word decoded in said migrant mode and the machine word decoded in said base mode (Shiell Abstract; column 1, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5);

h. Controlling the execution hardware units with said chosen machine word (Shiell column 3, lines 27-46; Figure 1; Figure 3a; Figure 3b; and Figure 5).

9. Shiell has not explicitly taught a VLIW architecture and simultaneously fetching from a memory a group of a plurality of instructions, each such group forming a fetch packet. However, Shiell has taught their system is usable with VLIW instruction sets (Shiell column 3, lines 36-42). However, Shiell has taught their system is usable with VLIW instruction sets (Shiell column 3, lines 36-42). O'Connor has taught a VLIW architecture comprising a base architecture and a migrant architecture (O'Connor column 1, line 9 to column 2, line 2) and simultaneously fetching from memory a group of a plurality of instructions, each such group forming a fetch packet (O'Connor column 1, line 9 to column 2, line 2). A person of ordinary skill in the art at the time the invention was would have recognized that using VLIW architecture improves code execution speed of the processor by executing more than one instruction simultaneously (O'Connor column 1, lines 16-17) and allowing more than one type of VLIW instruction set to run improves compatibility of the processor with other programs by expanding the number of very long instructions recognized (O'Connor column 1, lines 60-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW architecture and simultaneous fetching of O'Connor in Shiell to improve processor speed and compatibility.

10. Claims 2, 4-6, 8-9, 11, 13-15, and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell in view of O'Connor as applied to claims 1 and 10 above, and further in view of Nishioka et al., U.S. Patent Number 6,401,190 (herein referred to Nishioka).

11. Referring to claims 2, 4-9, Shiell has taught a VLIW architecture further comprising wherein said machine word controls the various types of execution hardware that evaluate functions on the operands to produce the results of said hardware execution units subsequent to said machine word controlling said local register files (Applicant's claim 6) (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5)

12. Shiell has not explicitly taught a VLIW architecture further comprising:

a. A third input to said multiplexer wherein said third input is a no operation instruction machine word (Applicant's claim 2);

b. Wherein said machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 4);

c. Wherein said machine word controls local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said machine word controlling said global register file (Applicant's claim 5);

d. Said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture (Applicant's claim 8); and

e. Wherein said VLIW architecture is a Digital signal Processor (DSP) (Applicant's claim 9).

13. However, Shiell has taught that the VLIW instruction set architecture is one of many possible instructions sets that can be used in the device (Shiell column 3, lines 36-42), but not the explicit details of the VLIW instruction set architecture. Nishioka has taught explicitly a VLIW architecture (Nishioka column1, line 41 to column 2, line 4) further comprising:

a. A third input to said multiplexer wherein said third input is a no operation instruction (Applicant's claim 2) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6);

b. Wherein said machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 4) (Nishioka column 4, lines 7-62);

c. Wherein said machine word controls local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said machine word controlling said global register file (Applicant's claim 5) (Nishioka column 4, lines 7-62);

d. Said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture (Applicant's claim 8) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6); and

e. Wherein said VLIW architecture is a Digital signal Processor (DSP) (Applicant's claim 9) (Nishioka column 1, lines 14-41).

14. A person of ordinary skill in the art at the time of applicant's invention would have recognized that a VLIW architecture simplifies hardware and how the hardware is controlled,

since no decoder is needed to translate the instruction from higher level instructions to machine level instructions is required (Nishioka column 1, lines 50-57). Hardware simplification would have motivated one of ordinary skill in the art to incorporate VLIW architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a VLIW architecture as taught by Nishioka in the device of Shiell to simplify hardware.

15. Referring to claims 11, 13-15, and 17-18, Shiell has taught a VLIW architecture method further comprising controlling the various types of execution hardware that evaluate functions on the operands to produce the results of said hardware execution units subsequent to controlling said local register files (Applicant's claim 15) (Shiell Abstract; column, line 61 to column 2, line 7; column 2, line 31 to column 3, line 14; column 7, line 19 to column 8, line 49; Figure 1; Figure 3a; Figure 3b; and Figure 5).

16. Shiell has not explicitly taught a VLIW architecture method further comprising:

a. Choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation instruction (Applicant's claim 11);

b. Controlling a global register file with said machine word, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 13);

c. Controlling local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said controlling said global register file (Applicant's claim 14);

d. Wherein said VLIW architecture is a Digital Signal Processor (DSP) (Applicant's claim 17); and

e. The step of issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture (Applicant's claim 18).

17. However, Shiell has taught that the VLIW instruction set architecture is one of many possible instructions sets that can be used in the device (Shiell column 3, lines 36-42), but not the specific details of the VLIW architecture. Nishioka has taught explicitly a VLIW architecture method (Nishioka column1, line 41 to column 2, line 4) further comprising:

a. Choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation instruction (Applicant's claim 11) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5, and Figure 6);

b. Controlling a global register file with said machine word, which supplies operands to all hardware execution units and accepts results of all hardware execution units (Applicant's claim 13) (Nishioka column 4, lines 7-62);

c. Controlling local register files that supply operands to either local execution hardware functional units or neighbor hardware execution functional units subsequent to said controlling said global register file (Applicant's claim 14) (Nishioka column 4, lines 7-62);

d. Wherein said VLIW architecture is a Digital Signal Processor (DSP) (Applicant's claim 17) (Nishioka column 1, lines 14-41); and

e. The step of issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture (Applicant's claim 18) (Nishioka column 7, lines 31-59; column 8, line 47 to column 9, line 20; column 14, lines 30-37; Figure 5; and Figure 6).

18. A person of ordinary skill in the art at the time of applicant's invention would have recognized that a VLIW architecture simplifies hardware and how the hardware is controlled, since no decoder is needed to translate the instruction from higher level instructions to machine level instructions is required (Nishioka column 1, lines 50-57). Hardware simplification would have motivated one of ordinary skill in the art to incorporate VLIW architecture. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a VLIW architecture as taught by Nishioka in the device of Shiell to simplify hardware.

Response to Arguments

19. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

20. In addition, the examiner has provided extrinsic evidence regarding the function of VLIW architecture, specifically to show that it is inherent that multiple instructions are fetched at once in VLIW architecture. Please see Hennessy and Patterson's Computer Architecture: A Quantitative Approach ©1996 page 284-285, section **The VLIW Approach**. As is explained in this section, VLIW architectures issue packets that contain multiple instructions that may be used

to operate functional units simultaneously in a single cycle. Consequently, multiple instructions are fetched simultaneously in one VLIW packet.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Mohamed et al., U.S. Patent Number 6,415,376, has taught VLIW architecture.

b. Tremblay et al., U.S. Patent Number 6,615,338, has taught VLIW architecture.

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

November 24, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100